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09/761,775	01/18/2001	Taisuke Sagara	088941/0178	5956

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EXAMINER	
TRAN, TRANG U	
ART UNIT	**PAPER NUMBER**
2614	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/761,775	SAGARA, TAISUKE	
	Examiner	Art Unit	
	Trang U. Tran	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,9,10 and 12-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,9,10 and 12-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 09, 2004 have been fully considered but they are not persuasive.

In re pages 10-11, applicant argues that in particular the cited portions of Aratani (nor the reminder of Aratani) simply do not disclose the vertical synchronization signals that are all synchronized with each other (unamended portion of claim 1, for example) nor does Aratani disclose the recited (amended of claim 1) non-display period provided between a common timing of each of said vertical synchronization signals and a timing of the image data, wherein said filter parameters are multiplexed with the decoded image data in the non-display period.

In response, the examiner respectfully disagrees. First of all, as discussed in the last Office Action, Aratani discloses in col. 4, lines 24-55, that "each input portion 2 receives from the **image source 1 not only the image data but also control signals to be used for reception of image data, such as a horizontal sync signal for line synchronization, a vertical sync signal for frame or field synchronization**, a clock signal for sampling each pixel, and a display enable signal indicating a transfer period of effective image data, each input portion 2 receives image data at an independent timing from other input portion", and also discloses in col. 5, lines 5-19, that **"the superposition data controller 8 controls to superpose image data different from that supplied from each input portion 2 on the display device 13**, reference numeral 10 represents a superposition data memory for storing data to be superposed,

reference numeral 11 represents an output display information conversion portion under the control of the bus controller 5 and for converting it into image data having a display format suitable for a display driving controller 12 which drives the display device 13, the display device 13 may be a CRT or a flat display panel (liquid crystal, plasma or the like) having a matrix electrode structure, the display device 13 may be a single display device **or a plurality of display devices**". From the above passage, it is clear that Aratani disclose the first feature is that vertical image synchronizing signals are generated synchronously, synchronized with each other and the non-display period provided between a common timing of each of said vertical synchronization signals and a timing of the image data. Such a structure makes it possible to synchronize images displayed on a plurality of monitors as recited in the amended independent claims 1, 2, 9, 10, 12 and 13.

Additionally, Aratani discloses in col. 6, lines 1-54 that "the input portion 2 which supplies the image source 1 with data such as **the numbers of dots, display lines, display colors, and a video output timing**" and in col. 7, lines 33-43, that "if the display device 13 is a TFT liquid crystal panel, this drive signal includes a line sync signal, a frame sync signal, an image data shift clock, image data, an alternating current signal and the like for driving a drive IC of the display device 13, if the display device is a CRT, **the display driving controller 12 converts the digital image data into analog R, G, and B image data and outputs them to the display device 13 together with the horizontal and vertical sync signals**". From the above passage, it is clear that Aratani does indeed disclose the newly added limitations "wherein said filter

parameters are multiplexed with the decoded image data in said non-display period.

Finally, as discussed in the last Office Action, Aratani also discloses in from col. 8, line 60 to col. 9, line 3, that "As shown in FIG. 2, consider the case while a first image (1-1) input from the image source 1-1 is displayed on the full screen of the display device, a second image (1-2) is input from the image source 1-2. In this case, there may be five or more display results of the images (1-1) and (1-2), including the display results of **(a), (b), (c), (d) and (e)**. Each display example can be realized by changing the display scaling at the display format conversion portions 3-1 and 3-2 and by changing the hierarchical level of the frame memory 9 having a priority order to the hierarchical level at which image data is stored". From the above passage, it is recognized that the **same image data** (1-1) or (1-2) can be converted into **five different predetermined formats as shown in (a), (b), (c), (d) and (e) in Fig. 2**. Thus, Aratani does indeed disclose the claimed the first feature is that **vertical image synchronizing signals are generated synchronously (Fig. 2e).**

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 9-10, 12-18, 20-24 and 26-31 are rejected under 35 U.S.C. 102(e) as

being anticipated by Aratani et al (US Patent No. 6,538,675 B2).

In considering claim 1, Aratani et al discloses all the claimed subject matter, note 1) the claimed a decoding device for converting input image coded data for generating and outputting image data by decoding said image coded data is met by the input portion 2 which has: an A/D converter and a PLL (phase locked loop) circuit for sampling image data if the input portion receives analog image data; **a decoder and a differential buffer if the input portion receives digital image data such LVDS (low voltage differential signaling)**; an encoder for encoding a composite signal into R, G and B signals if the input portion receives television or camcorder composite signals (Fig. 1, col. 4, line 16-41), or the encoder 201 to 204 which decodes television signals and the input portion 2 (Fig. 5, col. 12, lines 17-30), 2) the claimed a memory device for storing decoded image data generated by said decoding device is met by the input portion 2 which has: an A/D converter and a PLL (phase locked loop) circuit for sampling image data if the input portion receives analog image data; **a decoder and a differential buffer if the input portion receives digital image data such LVDS (low voltage differential signaling)**; or an encoder for encoding a composite signal into R, G and B signals if the input portion receives television or camcorder composite signals (Fig. 1, col. 4, line 16-41), 3) the claimed first to N-th (N being an integer 2 or more) image format conversion devices for generating first to N-th images by converting said decoded image data read from the memory device into respective predetermined image formats determined by input filter parameters, and outputting said first to N-th images in synchrony with input first to N-th vertical image synchronizing signals which are

synchronized with each other is met by **the display format conversion portions 3-1, 3-2, 3-3 and 3-4 and the control portion 6 supplies the conversion parameters to the display format conversion portions 3** (Figs. 1 and 2e, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38), 4) the claimed wherein a non-display period is provided between a common timing of each of said vertical image synchronizing signals and a timing of said image data is met by the display driving controller 12 (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43), and 5) the claimed wherein said filter parameters are multiplexed with the decoded image data in said non-display period is met by the input portion 2 which supplies the image source 1 with data such as the numbers of dots, display lines, display colors, and a video output timing (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43).

In considering claim 2, Aratani et al discloses all the claimed subject matter, note 1) the claimed first to N-th decoding devices which convert input first to N-th image coded data for generating and outputting first to N-th image data by decoding said first to N-th image coded data is met by the input portion 2 which has: an A/D converter and a PLL (phase locked loop) circuit for sampling image data if the input portion receives analog image data; **a decoder and a differential buffer if the input portion receives digital image data such LVDS (low voltage differential signaling)**; an encoder for encoding a composite signal into R, G and B signals if the input portion receives television or camcorder composite signals (Fig. 1, col. 4, line 16-41), or the encoder 201 to 204 which decodes television signals and the input portion 2 (Fig. 5, col. 12, lines 17-30), 2) the claimed a memory device for storing said first to N-th image data generated

by respective decoding devices is met by the input portion 2 which has: an A/D converter and a PLL (phase locked loop) circuit for sampling image data if the input portion receives analog image data; **a decoder and a differential buffer if the input portion receives digital image data such LVDS (low voltage differential signaling)**; or an encoder for encoding a composite signal into R, G and B signals if the input portion receives television or camcorder composite signals (Fig. 1, col. 4, line 16-41), 3) the claimed first to N-th image format conversion devices for generating first to N-th images by converting any of image data from among said first to N-th image data read from the memory device into respective predetermined image formats determined by input filter parameters, and outputting said first to N-th images in synchrony with input first to N-th vertical image synchronizing signals which are synchronized with each other is met by **the display format conversion portions 3-1, 3-2, 3-3 and 3-4 and the control portion 6 supplies the conversion parameters to the display format conversion portions 3** (Figs. 1 and 2e, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38), 4) the claimed wherein a non-display period is provided between a common timing of each of said vertical image synchronizing signals and a timing of said image data is met by the display driving controller 12 (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43), and 5) the claimed wherein said filter parameters are multiplexed with the decoded image data in said non-display period is met by the input portion 2 which supplies the image source 1 with data such as the numbers of dots, display lines, display colors, and a video output timing (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43).

In considering claim 3, the claimed wherein the image decoding apparatus comprises a distribution control apparatus for distributing any of the image data among said first to N-th image data respectively to first to N-th image format conversion devices, in response to a request of said first to N-th image format conversion device is met by the control portion 6 (Fig. 1, col. 4, line 56 to col. 5, lines 19).

In considering claim 9, Aratani et al discloses all the claimed subject matter, note 1) the claimed a decoding device for generating image data by decoding input image coded data, and for storing the thus generated image data in a memory device is met by the input portion 2 which has: an A/D converter and a PLL (phase locked loop) circuit for sampling image data if the input portion receives analog image data; **a decoder and a differential buffer if the input portion receives digital image data such LVDS (low voltage differential signaling)**; an encoder for encoding a composite signal into R, G and B signals if the input portion receives television or camcorder composite signals (Fig. 1, col. 4, line 16-41), or the encoder 201 to 204 which decodes television signals and the input portion 2 (Fig. 5, col. 12, lines 17-30), 2) the claimed a decoded data reading device for reading said image data stored in said memory device in response to an inputting decoded data request signal and for outputting said image data as decoded data is met by the control portion 6 (Fig. 1, col. 4, line 56 to col. 5, lines 19), 3) the claimed a first image format conversion device for generating a first image by converting said decoded data signal into a predetermined image format determined by input first filter parameter, and for outputting said first image in synchrony with an input first vertical image synchronizing signal is met by **the display format conversion portions**

3-1 and the control portion 6 supplies the conversion parameters to the display format conversion portions 3-1 (Figs. 1 and 2e, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38), 4) the claimed a second image format conversion device for generating a second image by converting said decoded data signal into a predetermined image format determined by an input second filter parameter, and for outputting said second image in synchrony with an input second vertical image synchronizing signal which is synchronized with said first vertical image synchronizing signal is met by reference numerals 3-2 represent a display format conversion portion (hereinafter called a "display format conversion portion 3") for converting a display format (the numbers of display lines, dots and colors) of image data received at the input portion 2-2, under control of a control portion 6 **and the control portion 6 supplies the conversion parameters to the display format conversion portions 3-2** (Figs. 1 and 2e, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38), 5) the claimed wherein a non-display period is provided between a common timing of each of said first and second vertical image synchronizing signals and a timing of said image data is met by the display driving controller 12 (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43), and 6) the claimed wherein said first and second filter parameters are multiplexed with the decoded image data in said non-display period is met by the input portion 2 which supplies the image source 1 with data such as the numbers of dots, display lines, display colors, and a video output timing (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43).

In considering claim 10, Aratani et al discloses all the claimed subject matter,

note 1) the claimed a first decoding device for generating a first image data by decoding input first image coded data and for storing the generated first image data in a memory device is met by the input portion 2-1 which has: an A/D converter and a PLL (phase locked loop) circuit for sampling image data if the input portion receives analog image data; **a decoder and a differential buffer if the input portion receives digital image data such LVDS (low voltage differential signaling)**; an encoder for encoding a composite signal into R, G and B signals if the input portion receives television or camcorder composite signals (Fig. 1, col. 4, line 16-41), or the encoder 201 to 204 which decodes television signals and the input portion 2 (Fig. 5, col. 12, lines 17-30), 2) the claimed a second decoding device for generating a second image data by decoding an input second image coded data, and for storing the generated second image data in the memory device is met by the input portion 2-2 which has: an A/D converter and a PLL (phase locked loop) circuit for sampling image data if the input portion receives analog image data; **a decoder and a differential buffer if the input portion receives digital image data such LVDS (low voltage differential signaling)**; an encoder for encoding a composite signal into R, G and B signals if the input portion receives television or camcorder composite signals (Fig. 1, col. 4, line 16-41), or the encoder 201 to 204 which decodes television signals and the input portion 2 (Fig. 5, col. 12, lines 17-30), 3) the claimed a decoded data reading device for reading said first or second image data stored in said memory device in response to an inputting first decoded data request signal and for reading said first or second image data stored in said memory device in response to an inputting second decoded data request signal and for

outputting said first and second image data is met by **the control portion 6** (Fig. 1, col. 4, line 56 to col. 5, lines 19), 4) the claimed a distribution control device for distributing said multiplexed decoded signal to a first decoded data signal corresponding to said first decoded data request signal and a second decoded data signal corresponding to said second decoded data request signal is met by **the control portion 6** (Fig. 1, col. 4, line 56 to col. 5, lines 19), 5) the claimed a first image format conversion device, which output the first decoded data request signal for generating a first image by converting said first decoded data signal into a first predetermined image format determined by an input first filter parameter and for outputting said first image in synchrony with an input first vertical image synchronizing signal is met by **the display format conversion portions 3-1 and the control portion 6 supplies the conversion parameters to the display format conversion portions 3-1** (Figs. 1 and 2e, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38), 6) the claimed a second image format conversion device which outputs the second decoded data request signal for generating a second image by converting said second decoded data signal into a second predetermined image format determined by an input second parameter, and for outputting said second image in synchrony with an input second vertical image synchronizing signal which is synchronized with said first vertical image synchronizing is met by reference numerals 3-2 represent a display format conversion portion (hereinafter called a "display format conversion portion 3") for converting a display format (the numbers of display lines, dots and colors) of image data received at the input portion 2-2, under control of a control portion 6 **and the control portion 6 supplies the conversion parameters to the**

display format conversion portions 3-2 (Figs. 1 and 2e, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38), 7) the claimed wherein a non-display period is provided between a common timing of each of said first and second vertical image synchronizing signals and a timing of said image data is met by the display driving controller 12 (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43), and 8) the claimed wherein said first and second filter parameters are multiplexed with the decoded image data in said non-display period is met by the input portion 2 which supplies the image source 1 with data such as the numbers of dots, display lines, display colors, and a video output timing (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43).

Claim 12 is rejected for the same reason as discussed in claim 9.

Claim 13 is rejected for the same reason as discussed in claim 10.

In considering claim 14, the claimed wherein said filter parameters are input to said first to N-th image format conversion devices in a predetermined period during which no decoded image data are input to said first to N-th image format conversion devices is met by **the control portion 6 which supplies the conversion parameters to the display format conversion portions 3** (Figs. 1 and 2, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38).

In considering claim 15, the claimed wherein said filter parameters are multiplexed with said decoded image data, and the multiplexed data are input to said first to N-th image format conversion devices is met by the digital television broadcast station which superposes control data, such as display image scaling and superposition

(Fig. 5, col. 12, lines 47-65).

In considering claim 16, the claimed wherein the non-display period includes a period between the time said vertical image synchronizing signals are input to said first to N-th image format conversion devices and the time said decoded image data are input to said first to N-th image format conversion devices is met by the input portion 2 which supplies the image source 1 with data such as the numbers of dots, display lines, display colors, and a video output timing (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43).

In considering claim 17, the claimed wherein said vertical image synchronizing signals are input to said first to N-th image format conversion devices at the same phase is met by **the control portion 6 which supplies the conversion parameters to the display format conversion portions 3** (Figs. 1 and 2, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38).

In considering claim 18, the claimed wherein said respective filter parameters are input to said first to N-th image format conversion devices in synchrony with said vertical image synchronizing signals corresponding thereto is met by **the control portion 6 which supplies the conversion parameters to the display format conversion portions 3** (Figs. 1 and 2, col. 4, lines 42-55 and col. 8, line 33 to col. 9, line 38).

Claims 20-24 are rejected for the same reason as discussed in claims 14-18, respectively.

Claim 26 is rejected for the same reason as discussed in claim 16.

Claim 27 is rejected for the same reason as discussed in claim 16.

Claim 28 is rejected for the same reason as discussed in claim 16.

In considering claim 29, the claimed wherein the non-display period includes a period between the time said vertical synchronizing signals are input to said first and second image format conversion devices and the time said image data are input to said first to N-th image format conversion devices is met by the input portion 2 which supplies the image source 1 with data such as the numbers of dots, display lines, display colors, and a video output timing (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43).

In considering claim 30, the claimed wherein the non-display period includes a period between the time said vertical synchronizing signals are input and the time said image data are input is met by the input portion 2 which supplies the image source 1 with data such as the numbers of dots, display lines, display colors, and a video output timing (Figs. 1 and 2e, col. 4, lines 42-55 and col. 6, line 1 to col. 7, line 43).

Claim 31 is rejected for the same reason as discussed in claim 30.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aratani et al (US Patent No. 6,538,675 B2) in view of Han (US Patent No. 6,175,387 B1).

In considering claim 5, Aratani et al discloses all the claimed subject matter, note 1) the claimed wherein the image decoding apparatus further comprises: an image synchronizing signal generation device for generating and outputting the first vertical image synchronizing signal used for outputting said image by any one of the image format conversion device among said first to N-th image format conversion devices is met by the input portions 2-1, 2-2, 2-3 and 2-4 (Fig. 1, col. 4, lines 8-41). However, Aratani et al explicitly does not disclose the claimed first to M-th (M: being an integer equal to N-1) image synchronizing signal generating and synchronization adjusting devices for generating and outputting the second to the N-th vertical image synchronizing signals respectively in synchronization with said first vertical image synchronizing signal used for outputting said images by said image format conversion devices other than said one of the image format conversion device. Han teaches that to interface the first video signal and the second video signal using the same port, a synchronization converter adjusts a difference between the sync signal of the second video signal to coincide with the sync signal of the first video signal and to correspond to the effective data (Fig. 4, col. 2, line 45 to col. 3, line 44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the a synchronization converter as taught by Han into Aratani et al's system in order to increase the flexibility of the system by providing the video system with video signals having different video formats.

In considering claim 6, the claimed wherein said first to M-th image synchronizing signal generating and synchronization adjusting devices comprise: a counter for

generating any one of said second to N-th vertical image synchronizing signals generated and output respectively by said first to M-th image synchronizing signal generating and synchronization adjusting devices and a counter control device for controlling the operation of said counter based on said first vertical image synchronizing signal is met by the sync converter 40 which includes a counter 42 counting synchronously with an external signal clock (Fig. 6, col. 3, line 59 to col. 4, line 44) of Han.

6. Claims 19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aratani et al (US Patent No. 6,538,675 B2) in view of the admitted prior art (Fig. 6).

In considering claim 19, Aratani et al disclose all the limitations of the instant invention, except for providing the claimed wherein said input image coded data is coded bit stream in MPEG form. The admitted prior art (Fig. 6) teach that Fig. 6 is block diagram showing the structure of the conventional image decoding apparatus, wherein the input coded data corresponding to coded bit stream in the form of the above MPEG (Fig. 6, page 2, line 1-25). Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the coded bit stream in MPEG form as taught by the admitted prior art (Fig. 6) into Aratani et al's system in order to reduce the bandwidth and size of the video signal to be transmitted.

Claim 25 is rejected for the same reason as discussed in claim 19.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (703) 305-0090. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TT TT
January 21, 2005

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600